BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated October 1, 2003. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

The Office Action acknowledged the non-receipt of the Priority documents filed on April 19, 2002. Applicants hereby attached a copy of the priority documents as well as the stamped receipt by the Patent Office. Applicants respectfully request the Examiner to trace the documents and indicate the status in the next office action.

Status of the Claims

Claims 81-84 are under consideration in this application. Claims 81 and 84 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention.

Additional Amendments

Claims 81 and 84 are being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejections

Claim 84 was objected to for an informality and requested correction thereof. As indicated, the claims have been amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 81-84 were rejected under 35 U.S.C. § 102(b) on the grounds of being anticipated by U.S. Pat. No. 5,656,550 to Tsuji et al. (hereinafter "Tsuji"), and claim 83 was rejected under

35 U.S.C. § 103(a) on the grounds of being unpatentable over Tsuji. These rejections have been carefully considered, but are most respectfully traversed.

The method of manufacturing a semiconductor device 1 of the invention (Figs. 98(a) – 98(g) and 99, a modification of Species (4), embodiment 23 described on pages 101-102), as now recited in claim 81, comprises the steps of: providing a metal substrate 20 having a front surface, a rear surface, first grooves on the front surface partitioning the front surface in parts, second grooves on the rear surface, each of the second grooves being arranged directly opposite to one of the first grooves 25 across the metal substrate 20 (p. 101, last paragraph); providing a semiconductor chip 5 having a front surface, a rear surface, electrodes 6 formed on the front surface; fixing the semiconductor chip 5 on the front surface of the metal substrate 20; forming a plurality of rows of external electrodes 2 **in** an area of the front surface of the metal substrate 20 and between an edge of the semiconductor chip 5 and an edge of the semiconductor device 1 (p. 16, 2nd to the last paragraph; Figs. 3 & 10); electrically connecting the electrodes 6 of the semiconductor chip with said external electrodes 2 formed in the front surface of the metal substrate 20 by conductive wires 7, respectively; forming a resin body 3a which seals the semiconductor chip 5, the conductive wires 7, and said external electrodes 2 formed in the front surface of the metal substrate 20; and after the resin body forming step, etching the rear surface of the metal substrate 20 so as to expose bottoms of the second grooves and electrically isolating said external electrodes 2 formed in the front surface of the metal substrate 20 from one another ("*isolate the partition regions [defined by the grooves]*" p.12, last 5 lines). As such, the semiconductor chip 5 (mounted "on/above" the substrate's front surface) is mounted on a level higher than the external electrodes 2 (formed "in/below" the substrate's front surface).

In a traditional semiconductor device having multi-row external electrodes in the narrow area between an edge of a semiconductor chip and an edge of the semiconductor device, such as the one disclosed in Fujimoto et al. (US 6498393; IDS reference filed on July 24, 2003), it is difficult to assure enough space between the external electrodes. Especially when the size of each external electrode is reduced, the mounting reliability (reliability when the semiconductor device is mounted on wiring substrate) reduces. However, according to the invention, the semiconductor chip 5 is mounted on a level higher than the one of the external electrodes 2 formed by the petition regions in the metal substrate 20. The provision of the external electrodes in the substrate (a level lower than the mounting surface of the semiconductor chip) is effective in assuring the mounting reliability as the size of each external electrode is reduced.

Applicants respectfully contend that none of the cited reference teaches or suggests "forming a plurality of rows of external electrodes 2 in an area of the front surface of the metal substrate 20 and between an edge of the semiconductor chip 5 and an edge of the semiconductor device 1" and "etching the rear surface of the metal substrate 20 so as to expose bottoms of the second grooves and electrically isolating said external electrodes 2 on the front surface of the metal substrate 20 from one another" of the invention.

Tsuji fails to disclose a semiconductor device having rows of external electrodes arranged in an area between an edge of a semiconductor chip and an edge of the semiconductor device. In addition, Tsjii's external electrodes 28 (Figs. 13B, 18B, 21B) are located *underneath* the semiconductor chip 41 (rather than *between an edge of the semiconductor chip 41 and an edge of the semiconductor device 21A*), although the external electrodes 28 are electrically isolating from one another. In the fifth embodiment of Tsuji depicted in Fig. 27, "the semiconductor device 90 is characterized in that **no** circuit substrate is provided in a package (col. 20, lines 25-27)" such that no external electrode provided in the substrate as in the present invention.

As mentioned, Fujimoto disclose a semiconductor device having rows of external electrodes arranged in an area between an edge of a semiconductor chip and an edge of the semiconductor device. However, Fujimoto's embodiment depicted in Figs. 2, 5F, 9F show that the chip 10 is mounted on the same surface as the external electrodes 11, rather than on a level higher than the one of the external electrodes 11. During the production process depicted in Figs. 5A, 14A, the chip 10 is mounted on a level *lower than* a top level of the external electrode constitution portions 15.

Applicants contend that one skilled in the art would not be motivated to combine the teachings in Tsuji and Fujimoto due to their conflicting external electrode arrangements with respect to the semiconductor chip. Tsuji's pole terminal portions 28 are arranged at the bottom side of the semiconductor chip 41 (col. 13, lines; Figs. 13B, 18B, 21B), which results in the top of the external electrodes being ***lower*** than the bottom of the semiconductor chip. On the other hand, Fujimoto prefers "*the top surface level of the semiconductor element 10 and the top surface level of the external electrode 11 are substantially the same* (col. 9, 2nd paragraph)." The top surface level of the external electrode 11 could be lower than the top surface level of the semiconductor element 10, but not lower than the bottom of the semiconductor element 10 (all Figs.). It is well established that any rejection based on combining conflicting teachings of the cited references is improper.

As such, the present invention as now claimed is distinguishable and thereby allowable over the rejection raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

January 2, 2004

SPF/JCM/JT

PATENT APPLICATION
(PENDING)

REED SMITH, LL[illegible] 3110[illegible] Review Park Drive, Suite 1400, Falls Church, VA 22042

Serial No.: 10/091,302 Filed: March 6, 2002 Atty Docket No: HITA-0176

Applicant(s): _____

DELIVER TO: ☐ MAIL ROOM ☐ ART UNIT: _____ ☐ _____

Special Instructions: _____

The PTO stamp hereon acknowledges receipt of:

- ☐ Amendment/Response
- ☐ Check - $_____
- ☐ Issue Fee Transmittal
- ☐ Assignment w/PTO-1595
- ☐ CPA Application under Rule 1.53(d)
- ☐ Extension of Time Petn. ☐
- ☐ Terminal Disclaimer
- ☐ __ Sheets of Drawings -- ☐ Formal ☐ Informal
- ☐ Small Entity Statements ☐ Inv. ☐ Sm. Bus. ☐ Non-Inv. ☐ Non-profit
- ☐ Missing Parts Response w/Decl
- ☐ Petition to Commissioner with fee
- ☒ Priority Document(s) 2
- ☐ Preliminary Amendment
- ☐ Information Discl. Stmt./refs.
- ☒ Notice of Priority
- ☐ Letter to Draftsman
- ☐ Notice of Appeal
- ☐ Appeal Brief (Triplicate)
- ☐ Reply Brief (Triplicate)
- ☐ Verified English Translation
- ☐ Revocation of Power of Attorney and Appointment of New Attorney
- ☐ Request for Refund
- ☐
- ☐

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of)
)
SHIMANUKI et al.)
)
Application Number: 10/091,302)
)
Filed: March 6, 2002)
)
For: A MANUFACTURING METHOD OF A SEMICONDUCTOR DEVICE)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

LETTER

Sir:

The below-identified communications are submitted in the above-captioned application or proceeding:

(X)	Priority Documents (2)	
(X)	Request for Priority	( ) Assignment Document
( )	Response to Missing Parts w/ signed Declaration	( ) Petition under 37 C.F.R. § 1.47(a)
		( ) Check for $

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication, including fees under 37 C.F.R. § 1.16 and 1.17 or credit any overpayment to **Deposit Account Number 08-1480**. A duplicate copy of this sheet is attached.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344
JUAN CARLOS A. MARQUEZ
Registration No. 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

April 18, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of)
)
SHIMANUKI et al.)
)
Application Number: 10/091,302)
)
Filed: March 6, 2002)
)
For: A MANUFACTURING METHOD OF A)
SEMICONDUCTOR DEVICE)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

REQUEST FOR PRIORITY
UNDER 35 U.S.C. § 119
AND THE INTERNATIONAL CONVENTION

Sir:

In the matter of the above-captioned application for a United States patent, notice is hereby given that the Applicant claims the priority dates of May 11, 2001 and January 11, 2002, the respective filing dates of the corresponding Japanese patent applications 2001-142164 and 2002-004435.

The certified copies of corresponding Japanese patent applications 2001-142164 and 2002-004435 are being submitted herewith. Acknowledgment of receipt of the certified copies is respectfully requested in due course.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

JUAN CARLOS A. MARQUEZ
Registration No. 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200
April 18, 2002

日　本　国　特　許　庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office

出願年月日
Date of Application: ２００１年　５月１１日

出願番号
Application Number: 特願２００１－１４２１６４

ST.10/C]: [ＪＰ２００１－１４２１６４]

出願人
Applicant(s): 株式会社日立製作所
日立米沢電子株式会社

２００２年　３月１９日

特許庁長官
Commissioner,
Japan Patent Office 及川耕造

日　本　国　特　許　庁
JAPAN　PATENT　OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されてハる事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office

出願年月日
Date of Application:　２００２年　１月１１日

出願番号
Application Number:　特願２００２－００４４３５

ST.10/C]:　[ＪＰ２００２－００４４３５]

出願人
Applicant(s):　株式会社日立製作所
日立米沢電子株式会社

２００２年　３月２２日

特許庁長官
Commissioner,
Japan Patent Office　及川耕造

出証番号　出証特２００２－３０１９６５７